IFW/DAC #

Patent Application
Attorney Docket No.: 57941.000063
Client Reference No.: RA001.2003.2.C.US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	:	
	:	
Michael Farmwald et al.	:	Group Art Unit: 2818
	:	
Appln. No.: 10/716,596	:	
	:	Examiner: unassigned
Filed: November 20, 2003	:	
	:	
For: Controller Device And Method Of Operating Same (As Amended)	:	

Mail Stop Petition
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PETITION UNDER 37 CFR § 1.182

Sir:

In response to the Notice of Omitted Items dated August 9, 2004 (a copy of which is attached hereto), Applicants hereby petition the Commissioner for Patents to accept pages 1-17 of the specification of the above-referenced patent application (copies of which are attached hereto). It is respectfully submitted that these pages were previously submitted to the U.S. Patent and Trademark Office (USPTO) at the time of filing the above-referenced patent application (i.e., on November 20, 2003). Evidence of such previous submission include: 1.) a copy of the Request For Filing A Continuation Patent Application Under 37 CFR 1.53(b), which was filed with the above-referenced patent application on November 20, 2003, listing the total

number of pages contained in the specification of the above-referenced patent application (a copy of which is attached hereto); and 2.) a date-stamped Return Receipt Post Card, which was filed with the above-referenced patent application on November 20, 2003, listing the total number of pages contained in the specification of the above-referenced patent application (a copy of which is attached hereto).

Please charge the petition fee in the amount of $130.00 to Deposit Account No. 50-0206. Also, please credit the refund of the petition fee to Deposit Account No. 50-0206.

Please also charge any shortage in fees due in connection with the filing of this communication to Deposit Account No. 50-0206, and please credit any excess fees to such deposit account.

To the extent necessary, a petition for an extension of time under 37 CFR § 1.136 is hereby made.

Respectfully submitted,

Hunton & Williams LLP

By: _____
Thomas E. Anderson
Registration No. 37,063

TEA/vrp

Hunton & Williams LLP
1900 K Street, N.W.
Washington, D.C. 20006-1109
Telephone: (202) 955-1500
Facsimile: (202) 778-2201

Date: August 17, 2004

UTILITY ☒ DESIGN ☐

Application Serial No.: **Unassigned**
Inventor: **Michael FARMWALD, et al.**
Filing Date: **November 20, 2003**
Atty/Sec.: **TEA/mia**

Client/Matter: **57941.000063**
Client: **Rambus Inc.**

Date: November 20, 2003

Title: **INTEGRATED CIRCUIT I/O USING A HIGH PERFORMANCE BUS INTERFACE**

The following has been received in the U.S. Patent and Trademark Office on the date stamped hereon:

1. *Request for Filing a Continuation Patent Application Transmittal*
2. *Copy of Specifcation, (125 pages); 14 pages of drawings; and Declaration and Power of Attorney (2 pages)*
3. *Postcard Receipt*
4. *Check in the amount of $770.00*
5. *This application is a Continuation Application of 10/037.171, filed on 12/21/01 (Our File No. 57941.000027)*

4/18/90

REQUEST FOR FILING A CONTINUATION PATENT APPLICATION UNDER 37 CFR 1.53(b)

Attorney Docket No: 57941.000063
Client Reference No.: RA001.2003.2.C.US

Pending Prior U.S. Patent Application No.: 10/037,171
Prior Art Unit: 2181
Prior Examiner: G. Auve'

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is a request for filing a continuation patent application under 37 CFR 1.53(b) of pending prior U.S. Patent Application No. 10/037,171, filed on December 21, 2001, entitled, INTEGRATED CIRCUIT I/O USING A HIGH PERFORMANCE BUS INTERFACE, by the below-named inventor(s):

INVENTOR	RESIDENCE	CITIZENSHIP	POST OFFICE ADDRESS
Michael FARMWALD	Berkeley, CA	U.S.A.	82 Eucalyptus Road, Berkeley, California 94705
Mark HOROWITZ	Palo Alto, CA	U.S.A.	2024 Columbia Street, Palo Alto, California 94306

1. [X] Attached is a copy of the executed oath or declaration in pending prior U.S. Patent Application No. 10/037,171, showing the original signature(s) or an indication that it was signed. The entire disclosure of pending prior U.S. Patent Application No. 10/037,171, from which the copy of the executed oath or declaration is supplied, is considered a part of the disclosure of the present patent application and is hereby incorporated herein by reference.

2. [X] 125 pages of specification; 2 pages of declaration; and 14 sheets of informal drawings are attached. No new matter has been added.

3. [ ] A signed statement is attached deleting inventor(s) named in the above-identified pending prior patent application (see 37 CFR 1.63(d)(2) and 1.33(b)).

4. [X] Please cancel claims 2-150.

5. [ ] A Preliminary Amendment is attached.

6. [ ] The present patent application is entitled to small entity status.

7. [X] The filing fee is calculated below on the basis of the claims existing in the present patent application, as amended at 4 and 5 above (if applicable):

	# of Claims		Extra Claims	Rate	Fee
Total Claims	1	Minus 20	0	x $.00	$.00
Independent Claims	0	Minus 3	0	x $.00	$.00
Basic Application Fee					$770.00
If multiple dependent claims are present, add $280.00					N/A
Subtotal					$770.00
Subtract ½ if small entity					N/A
Total Application Fee					$770.00
TOTAL FEE DUE					$770.00

8. [ ] Please charge Deposit Account No. 50-0206 in the amount of $.00 for the above-indicated fees. A duplicate copy of this transmittal is submitted herewith.

9. [X] The Commissioner is hereby authorized to charge any shortage in fees under 37 CFR 1.16 and 1.17 associated with the filing of the present patent application,

including any extension of time fees to maintain the pendency of prior U.S. Patent Application No. _____, or credit any overpayment, to Deposit Account No. 50-0206. A duplicate copy of this transmittal is submitted herewith.

10. [X] The Commissioner is hereby authorized to charge any shortage in fees under 37 CFR 1.16 and 1.17 which are required during the pendency of the present patent application, or credit any overpayment, to Deposit Account No. 50-0206. This authorization does not include any issue fees under 37 CFR 1.18. A duplicate copy of this transmittal is submitted herewith.

11. [ ] Priority of foreign Application No. _____, filed on _____, in _____, is claimed under 35 USC 119. The certified priority document(s) were filed in U.S. Patent Application No. _____, filed on _____.

12. [X] The above-identified pending prior patent application is assigned of record to: RAMBUS INC.

13. [X] The power of attorney in the above-identified pending prior patent application is to:

Thomas E. Anderson et al.
Hunton & Williams LLP
1900 K Street, N.W.
Washington, D.C. 20006-1109

14. [X] Address all future communications to:

Thomas E. Anderson
Hunton & Williams LLP
1900 K Street, N.W.
Washington, D.C. 20006-1109
Customer No.: 2197

15. [X] A return receipt postcard is submitted herewith.

16. [ ] Also attached: Request and Certification under 35 USC 122(b)(2).

It is understood that secrecy under 35 USC 122 is hereby waived to the extent that if information or access is available under 37 CFR 1.14 to any one of the applications in the file wrapper of a 37 CFR 1.53(b) application, be it either this application or a prior application in the same file wrapper, the Patent and Trademark Office may provide similar information or access to all the other applications in the same file wrapper.

Respectfully submitted,

Hunton & Williams LLP

BY: _____
Thomas E. Anderson
Registration No. 37,063

TEA/mia

Hunton & Williams LLP
1900 K Street, N.W.
Washington, D.C. 20006-1109
Telephone: (202) 955-1500
Facsimile: (202) 778-2201

Date: November 20, 2003

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
10/716,596	11/20/2003	Michael Farmwald	57941.000063

CONFIRMATION NO. 7201

Thomas E. Anderson
Hunton & Williams LLP
1900 K Street, N.W.
Washington, DC 20006-1109

FORMALITIES LETTER

OC000000013485490

Date Mailed: 08/09/2004

NOTICE OF OMITTED ITEM(S) IN A NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

A filing date has been accorded to the above-identified nonprovisional application papers; however, the following item(s) appear to have been omitted from the application:

- Page(s) **1-17** of the specification (description and claims).

I. Should applicant contend that the above-noted omitted item(s) was in fact deposited in the U.S. Patent and Trademark Office (USPTO) with the nonprovisional application papers, a copy of this Notice and a petition (and $130.00 petition fee *(37 CFR 1.17(h))*) with evidence of such deposit **must** be filed within **TWO MONTHS** of the date of this Notice. The petition fee will be refunded if is determined that the item(s) was received by the USPTO.

II. Should applicant desire to supply the omitted item(s) and accept the date that such omitted item(s) was filed in the USPTO as the filing date of the above-identified application, a copy of this Notice, the omitted item(s) (with a supplemental oath or declaration in compliance with 37 CFR 1.63 and 1.64 referring to such items), and a petition under 37 CFR 1.182 (with the $130.00 petition fee *(37 CFR 1.17(h))* requesting the later filing date **must** be filed within **TWO MONTHS** of the date of this Notice.

Applicant is advised that generally the filing fee required for an application is the filing fee in effect on the filing date accorded the application and that payment of the requisite basic filing fee on a date later than the filing date of the application requires payment of a surcharge (37 CFR 1.16(e)). To avoid processing delays and payment of a surcharge, applicant should submit any balance due for the requisite filing fee based on the later filing date being requested when submitting the omitted items(s) and the petition (and petition fee) requesting the later filing date.

III. The failure to file a petition (and petition fee) under the above options (I) or (II) within **TWO MONTHS** of the date of this Notice (37 CFR 1.181(f)) will be treated as a constructive acceptance by the applicant of the application as deposited in the USPTO. **THIS TWO MONTH PERIOD IS NOT EXTENDABLE UNDER 37 CFR 1.136(a) or (b)**. In the absence of a timely filed petition in reply to this Notice, the application will maintain a filing date as of the date of deposit of the application papers in the USPTO, and original application papers (*i.e.*, the original disclosure of the invention) will include only those application papers present in the USPTO on the date of deposit.

In the event that applicant elects not to take action pursuant to options (I) or (II) above (thereby constructively electing option (III)), amendment of the specification to renumber the pages consecutively and cancel incomplete sentences caused by any omitted page(s), and/or amendment of the specification to cancel all references to any omitted drawing(s), relabel the drawing figures to be numbered consecutively (if necessary), and correct the

references in the specification to the drawing figures to correspond with any relabeled drawing figures, is required. A copy of the drawing figures showing the proposed changes in red ink should accompany with any drawing changes . Such amendment and/or correction to the drawing figures, if necessary, should be by way of preliminary amendment submitted prior to the first Office action to avoid delays in the prosecution of the application.

Replies should be mailed to: Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

A copy of this notice MUST be returned with the reply.

Customer Service Center
Initial Patent Examination Division (703) 308-1202
PART 2 - COPY TO BE RETURNED WITH RESPONSE

Our Ref: RamBus D-1

Integrated Circuit I/O Using A High Performance Bus Interface

FIELD OF THE INVENTION

An integrated circuit bus interface for computer and video systems is described which allows high speed transfer of blocks of data, particularly to and from memory devices, with reduced power consumption and increased system reliability. A new method of physically implementing the bus architecture is also described.

BACKGROUND OF THE INVENTION

Semiconductor computer memories have traditionally been designed and structured to use one memory device for each bit, or small group of bits, of any individual computer word, where the word size is governed by the choice of computer. Typical word sizes range from 4 to 64 bits. Each memory device typically is connected in parallel to a series of address lines and connected to one of a series of data lines. When the computer seeks to read from or write to a specific memory location, an address is put on the address lines and some or all of the memory devices are activated using a separate device select line for each needed device. One or more devices may be connected to each data line but typically only a small number of data lines are connected to

a single memory device. Thus data line 0 is connected to device(s) 0, data line 1 is connected to device(s) 1, and so on. Data is thus accessed or provided in parallel for each memory read or write operation. For the system to operate properly, every single memory bit in every memory device must operate dependably and correctly.

To understand the concept of the present invention, it is helpful to review the architecture of conventional memory devices. Internal to nearly all types of memory devices (including the most widely used Dynamic Random Access Memory (DRAM), Static RAM (SRAM) and Read Only Memory (ROM) devices), a large number of bits are accessed in parallel each time the system carries out a memory access cycle. However, only a small percentage of accessed bits which are available internally each time the memory device is cycled ever make it across the device boundary to the external world.

Referring to Fig. 1, all modern DRAM, SRAM and ROM designs have internal architectures with row (word) lines 5 and column (bit) lines 6 to allow the memory cells to tile a two dimensional area 1. One bit of data is stored at the intersection of each word and bit line. When a particular word line is enabled, all of the corresponding data bits are transferred onto the bit lines. Some prior art DRAMs take advantage of this organization to reduce the number of pins needed to transmit the address. The address of a given memory

cell is split into two addresses, row and column, each of which can be multiplexed over a bus only half as wide as the memory cell address of the prior art would have required.

COMPARISON WITH PRIOR ART

Prior art memory systems have attempted to solve the problem of high speed access to memory with limited success. U.S. Patent No. 3,821,715 (Hoff et. al.), was issued to Intel Corporation for the earliest 4-bit micro-processor. That patent describes a bus connecting a single central processing unit (CPU) with multiple RAMs and ROMs. That bus multiplexes addresses and data over a 4-bit wide bus and uses point-to-point control signals to select particular RAMs or ROMs. The access time is fixed and only a single processing element is permitted. There is no block-mode type of operation, and most important, not all of the interface signals between the devices are bused (the ROM and RAM control lines and the RAM select lines are point-to-point).

In U.S. Patent No. 4,315,308 (Jackson), a bus connecting a single CPU to a bus interface unit is described. The invention uses multiplexed address, data, and control information over a single 16-bit wide bus. Block-mode operations are defined, with the length of the block sent as part of the control sequence. In addition, variable access-time operations using a "stretch" cycle signal are provided. There are no

multiple processing elements and no capability for multiple outstanding requests, and again, not all of the interface signals are bused.

In U.S. Patent No. 4,449,207 (Kung, et. al.), a DRAM is described which multiplexes address and data on an internal bus. The external interface to this DRAM is conventional, with separate control, address and data connections.

In U.S. Patent Nos. 4,764,846 and 4,706,166 (Go), a 3-D package arrangement of stacked die with connections along a single edge is described. Such packages are difficult to use because of the point-to-point wiring required to interconnect conventional memory devices with processing elements. Both patents describe complex schemes for solving these problems. No attempt is made to solve the problem by changing the interface.

In U.S. Patent No. 3,969,706 (Proebsting, et. al.), the current state-of-the-art DRAM interface is described. The address is two-way multiplexed, and there are separate pins for data and control (RAS, CAS, WE, CS). The number of pins grows with the size of the DRAM, and many of the connections must be made point-to-point in a memory system using such DRAMs.

There are many backplane buses described in the prior art, but not in the combination described or having the features of this invention. Many backplane buses multiplex addresses and data on a single bus (e.g., the NU bus). ELXSI and others have implemented split-transaction buses (U.S. Patent No. 4,595,923

and 4,481,625 (Roberts)). ELXSI has also implemented a relatively low-voltage-swing current-mode ECL driver (approximately 1 V swing). Address-space registers are implemented on most backplane buses, as is some form of block mode operation.

Nearly all modern backplane buses implement some type of arbitration scheme, but the arbitration scheme used in this invention differs from each of these. U.S. Patent Nos. 4,837,682 (Culler), 4,818,985 (Ikeda), 4,779,089 (Theus) and 4,745,548 (Blahut) describe prior art schemes. All involve either log N extra signals, (Theus, Blahut), where N is the number of potential bus requestors, or additional delay to get control of the bus (Ikeda, Culler). None of the buses described in patents or other literature use only bused connections. All contain some point-to-point connections on the backplane. None of the other aspects of this invention such as power reduction by fetching each data block from a single device or compact and low-cost 3-D packaging even apply to backplane buses.

The clocking scheme used in this invention has not been used before and in fact would be difficult to implement in backplane buses due to the signal degradation caused by connector stubs. U.S. Patent No. 4,247,817 (Heller) describes a clocking scheme using two clock lines, but relies on ramp-shaped clock signals in contrast to the normal rise-time signals used in the present invention.

In U.S. Patent No. 4,646,279 (Voss), a video RAM is described which implements a parallel-load, serial-out shift register on the output of a DRAM. This generally allows greatly improved bandwidth (and has been extended to 2, 4 and greater width shift-out paths.) The rest of the interfaces to the DRAM (RAS, CAS, multiplexed address, etc.) remain the same as for conventional DRAMS.

One object of the present invention is to use a new bus interface built into semiconductor devices to support high-speed access to large blocks of data from a single memory device by an external user of the data, such as a microprocessor, in an efficient and cost-effective manner.

Another object of this invention is to provide a clocking scheme to permit high speed clock signals to be sent along the bus with minimal clock skew between devices.

Another object of this invention is to allow mapping out defective memory devices or portions of memory devices.

Another object of this invention is to provide a method for distinguishing otherwise identical devices by assigning a unique identifier to each device.

Yet another object of this invention is to provide a method for transferring address, data and control information over a relatively narrow bus and to provide a method of bus arbitration when multiple devices seek to use the bus simultaneously.

Another object of this invention is to provide a method of distributing a high-speed memory cache within the DRAM chips of a memory system which is much more effective than previous cache methods.

Another object of this invention is to provide devices, especially DRAMs, suitable for use with the bus architecture of the invention.

SUMMARY OF INVENTION

The present invention includes a memory subsystem comprising at least two semiconductor devices, including at least one memory device, connected in parallel to a bus, where the bus includes a plurality of bus lines for carrying substantially all address, data and control information needed by said memory devices, where the control information includes device-select information and the bus has substantially fewer bus lines than the number of bits in a single address, and the bus carries device-select information without the need for separate device-select lines connected directly to individual devices.

Referring to Fig. 2, a standard DRAM 13, 14, ROM (or SRAM) 12, microprocessor CPU 11, I/O device, disk controller or other special purpose device such as a high speed switch is modified to use a wholly bus-based interface rather than the prior art combination of point-to-point and bus-based wiring used with conventional versions of these devices. The new bus

includes clock signals, power and multiplexed address, data and control signals. In a preferred implementation, 8 bus data lines and an AddressValid bus line carry address, data and control information for memory addresses up to 40 bits wide. Persons skilled in the art will recognize that 16 bus data lines or other numbers of bus data lines can be used to implement the teaching of this invention. The new bus is used to connect elements such as memory, peripheral, switch and processing units.

In the system of this invention, DRAMs and other devices receive address and control information over the bus and transmit or receive requested data over the same bus. Each memory device contains only a single bus interface with no other signal pins. Other devices that may be included in the system can connect to the bus and other non-bus lines, such as input/output lines. The bus supports large data block transfers and split transactions to allow a user to achieve high bus utilization. This ability to rapidly read or write a large block of data to one single device at a time is an important advantage of this invention.

The DRAMs that connect to this bus differ from conventional DRAMs in a number of ways. Registers are provided which may store control information, device identification, device-type and other information appropriate for the chip such as the address range for each independent portion of the device. New bus interface circuits must be added and the internals of

prior art DRAM devices need to be modified so they can provide and accept data to and from the bus at the peak data rate of the bus. This requires changes to the column access circuitry in the DRAM, with only a minimal increase in die size. A circuit is provided to generate a low skew internal device clock for devices on the bus, and other circuits provide for demultiplexing input and multiplexing output signals.

High bus bandwidth is achieved by running the bus at a very high clock rate (hundreds of MHz). This high clock rate is made possible by the constrained environment of the bus. The bus lines are controlled-impedance, doubly-terminated lines. For a data rate of 500 MHz, the maximum bus propagation time is less than 1 ns (the physical bus length is about 10 cm). In addition, because of the packaging used, the pitch of the pins can be very close to the pitch of the pads. The loading on the bus resulting from the individual devices is very small. In a preferred implementation, this generally allows stub capacitances of 1-2 pF and inductances of 0.5 - 2 nH. Each device 15, 16, 17, shown in Figure 3, only has pins on one side and these pins connect directly to the bus 18. A transceiver device 19 can be included to interface multiple units to a higher order bus through pins 20.

A primary result of the architecture of this invention is to increase the bandwidth of DRAM access. The invention also

reduces manufacturing and production costs, power consumption, and increases packing density and system reliability.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a diagram which illustrates the basic 2-D organization of memory devices.

Figure 2 is a schematic block diagram which illustrates the parallel connection of all bus lines and the serial Reset line to each device in the system.

Figure 3 is a perspective view of a system of the invention which illustrates the 3-D packaging of semiconductor devices on the primary bus.

Figure 4 shows the format of a request packet.

Figure 5 shows the format of a retry response from a slave.

Figure 6 shows the bus cycles after a request packet collision occurs on the bus and how arbitration is handled.

Figure 7 shows the timing whereby signals from two devices can overlap temporarily and drive the bus at the same time.

Figure 8 shows the connection and timing between bus clocks and devices on the bus.

Figure 9 is a perspective view showing how transceivers can be used to connect a number of bus units to a transceiver

bus. Figure 10 is a block and schematic diagram of input/output circuitry used to connect devices to the bus.

Figure 11 is a schematic diagram of a clocked sense-amplifier used as a bus input receiver.

Figure 12 is a block diagram showing how the internal device clock is generated from two bus clock signals using a set of adjustable delay lines.

Figure 13 is a timing diagram showing the relationship of signals in the block diagram of Figure 12.

Figure 14 is timing diagram of a preferred means of implementing the reset procedure of this invention.

Figure 15 is a diagram illustrating the general organization of a 4 Mbit DRAM divided into 8 subarrays.

DETAILED DESCRIPTION

The present invention is designed to provide a high speed, multiplexed bus for communication between processing devices and memory devices and to provide devices adapted for use in the bus system. The invention can also be used to connect processing devices and other devices, such as I/O interfaces or disk controllers, with or without memory devices on the bus. The bus consists of a relatively small number of lines connected in parallel to each device on the bus. The bus carries substantially all address, data and control information needed by devices for communication with other devices on the bus. In many

systems using the present invention, the bus carries almost every signal between every device in the entire system. There is no need for separate device-select lines since device-select information for each device on the bus is carried over the bus. There is no need for separate address and data lines because address and data information can be sent over the same lines. Using the organization described herein, very large addresses (40 bits in the preferred implementation) and large data blocks (1024 bytes) can be sent over a small number of bus lines (8 plus one control line in the preferred implementation).

Virtually all of the signals needed by a computer system can be sent over the bus. Persons skilled in the art recognize that certain devices, such as CPUs, may be connected to other signal lines and possibly to independent buses, for example a bus to an independent cache memory, in addition to the bus of this invention. Certain devices, for example cross-point switches, could be connected to multiple, independent buses of this invention. In the preferred implementation, memory devices are provided that have no connections other than the bus connections described herein and CPUs are provided that use the bus of this invention as the principal, if not exclusive, connection to memory and to other devices on the bus.

All modern DRAM, SRAM and ROM designs have internal architectures with row (word) and column (bit) lines to efficiently tile a 2-D area. Referring to Fig. 1, one bit of

data is stored at the intersection of each word line 5 and bit line 6. When a particular word line is enabled, all of the corresponding data bits are transferred onto the bit lines. This data, about 4000 bits at a time in a 4 MBit DRAM, is then loaded into column sense amplifiers 3 and held for use by the I/O circuits.

In the invention presented here, the data from the sense amplifiers is enabled 32 bits at a time onto an internal device bus running at approximately 125 MHz. This internal device bus moves the data to the periphery of the devices where the data is multiplexed into an 8-bit wide external bus interface, running at approximately 500 MHz.

The bus architecture of this invention connects master or bus controller devices, such as CPUs, Direct Memory Access devices (DMAs) or Floating Point Units (FPUs), and slave devices, such as DRAM, SRAM or ROM memory devices. A slave device responds to control signals; a master sends control signals. Persons skilled in the art realize that some devices may behave as both master and slave at various times, depending on the mode of operation and the state of the system. For example, a memory device will typically have only slave functions, while a DMA controller, disk controller or CPU may include both slave and master functions. Many other semiconductor devices, including I/O devices, disk controllers, or other special purpose devices

such as high speed switches can be modified for use with the bus of this invention.

Each semiconductor device contains a set of internal registers, preferably including a device identification (device ID) register, a device-type descriptor register, control registers and other registers containing other information relevant to that type of device. In a preferred implementation, semiconductor devices connected to the bus contain registers which specify the memory addresses contained within that device and access-time registers which store a set of one or more delay times at which the device can or should be available to send or receive data.

Most of these registers can be modified and preferably are set as part of an initialization sequence that occurs when the system is powered up or reset. During the initialization sequence each device on the bus is assigned a unique device ID number, which is stored in the device ID register. A bus master can then use these device ID numbers to access and set appropriate registers in other devices, including access-time registers, control registers, and memory registers, to configure the system. Each slave may have one or several access-time registers (four in a preferred embodiment). In a preferred embodiment, one access-time register in each slave is permanently or semi-permanently programmed with a fixed value to facilitate

certain control functions. A preferred implementation of an initialization sequence is described below in more detail.

All information sent between master devices and slave devices is sent over the external bus, which, for example, may be 8 bits wide. This is accomplished by defining a protocol whereby a master device, such as a microprocessor, seizes exclusive control of the external bus (i.e., becomes the bus master) and initiates a bus transaction by sending a request packet (a sequence of bytes comprising address and control information) to one or more slave devices on the bus. An address can consist of 16 to 40 or more bits according to the teachings of this invention. Each slave on the bus must decode the request packet to see if that slave needs to respond to the packet. The slave that the packet is directed to must then begin any internal processes needed to carry out the requested bus transaction at the requested time. The requesting master may also need to transact certain internal processes before the bus transaction begins. After a specified access time the slave(s) respond by returning one or more bytes (8 bits) of data or by storing information made available from the bus. More than one access time can be provided to allow different types of responses to occur at different times.

A request packet and the corresponding bus access are separated by a selected number of bus cycles, allowing the bus to be used in the intervening bus cycles by the same or other

masters for additional requests or brief bus accesses. Thus multiple, independent accesses are permitted, allowing maximum utilization of the bus for transfer of short blocks of data. Transfers of long blocks of data use the bus efficiently even without overlap because the overhead due to bus address, control and access times is small compared to the total time to request and transfer the block.

Device Address Mapping

Another unique aspect of this invention is that each memory device is a complete, independent memory subsystem with all the functionality of a prior art memory board in a conventional backplane-bus computer system. Individual memory devices may contain a single memory section or may be subdivided into more than one discrete memory section. Memory devices preferably include memory address registers for each discrete memory section. A failed memory device (or even a subsection of a device) can be "mapped out" with only the loss of a small fraction of the memory, maintaining essentially full system capability. Mapping out bad devices can be accomplished in two ways, both compatible with this invention.

The preferred method uses address registers in each memory device (or independent discrete portion thereof) to store information which defines the range of bus addresses to which this memory device will respond. This is similar to prior art

schemes used in memory boards in conventional backplane bus systems. The address registers can include a single pointer, usually pointing to a block of known size, a pointer and a fixed or variable block size value or two pointers, one pointing to the beginning and one to the end (or to the "top" and "bottom") of each memory block. By appropriate settings of the address registers, a series of functional memory devices or discrete memory sections can be made to respond to a contiguous range of addresses, giving the system access to a contiguous block of good memory, limited primarily by the number of good devices connected to the bus. A block of memory in a first memory device or memory section can be assigned a certain range of addresses, then a block of memory in a next memory device or memory section can be assigned addresses starting with an address one higher (or lower, depending on the memory structure) than the last address of the previous block.

Preferred devices for use in this invention include device-type register information specifying the type of chip, including how much memory is available in what configuration on that device. A master can perform an appropriate memory test, such as reading and writing each memory cell in one or more selected orders, to test proper functioning of each accessible discrete portion of memory (based in part on information like device ID number and device-type) and write address values (up to 40 bits in the preferred embodiment, 10^{12} bytes), preferably